

-20V, -0.7A, 394mΩ P-channel Power Trench MOSFET

JMTL3139KT5

Features

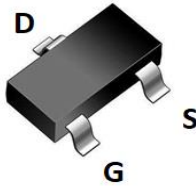
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Halogen-free; RoHS-compliant
- Pb-free plating

Applications

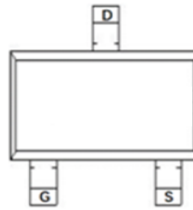
- Load Switch
- PWM Application
- Power Management

Product Summary

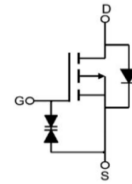
Parameters	Value	Unit
V_{DSS}	-20	V
$V_{GS(th_Typ)}$	-0.7	V
$I_D(@V_{GS}=10V)$	-0.7	A
$R_{DS(ON_Typ)}(@V_{GS}=-4.5V)$	307	mΩ
$R_{DS(ON_Typ)}(@V_{GS}=-2.5V)$	394	mΩ



SOT-523-3L Top View



Pin Assignment



Schematic Diagram

Ordering Information

Device	Marking	MSL	Form	Package	Reel(pcs)	Per Carton (pcs)
JMTL3139KT5	39K	3	Tape&Reel	SOT-523-3L	3000	120000

Absolute Maximum Ratings (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-to-Source Voltage	-20	V
V_{GS}	Gate-to-Source Voltage	± 10	V
I_D	Continuous Drain Current	$T_A = 25^\circ\text{C}$	-0.7
		$T_A = 100^\circ\text{C}$	-0.4
I_{DM}	Pulsed Drain Current ⁽¹⁾	Refer to Fig.4	A
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$	0.5
		$T_A = 100^\circ\text{C}$	0.1
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽²⁾	412	



Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$	-20	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -20\text{V}, V_{GS} = 0\text{V}$	-	-	-1.0	μA
I_{GSS}	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 10\text{V}$	-	-	± 10	μA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-0.5	-0.7	-0.9	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance ⁽³⁾	$V_{GS} = -4.5\text{V}, I_D = -0.5\text{A}$	-	307	399	$\text{m}\Omega$
		$V_{GS} = -2.5\text{V}, I_D = -0.4\text{A}$	-	394	600	$\text{m}\Omega$
Dynamic Characteristics						
R_g	Gate Resistance	$f = 1\text{MHz}$	-	174	-	Ω
C_{iss}	Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = -10\text{V}, f = 1\text{MHz}$	-	70	-	pF
C_{oss}	Output Capacitance		-	18	-	pF
C_{rss}	Reverse Transfer Capacitance		-	10	-	pF
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ to } -4.5\text{V}$ $V_{DS} = -10\text{V}, I_D = -1\text{A}$	-	1.0	-	nC
Q_{gs}	Gate Source Charge		-	0.3	-	nC
Q_{gd}	Gate Drain("Miller") Charge		-	0.1	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On DelayTime	$V_{GS} = -4.5\text{V}, V_{DD} = -10\text{V}$ $I_D = -0.5\text{A}, R_{GEN} = 3\Omega$	-	6.2	-	ns
t_r	Turn-On Rise Time		-	7.3	-	ns
$t_{d(off)}$	Turn-Off DelayTime		-	40	-	ns
t_f	Turn-Off Fall Time		-	22	-	ns
Body Diode Characteristics						
I_S	Maximum Continuous Body Diode Forward Current		-	-	-0.7	A
I_{SM}	Maximum Pulsed Body Diode Forward Current		-	-	-2.8	A
V_{SD}	Body Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = -0.5\text{A}$	-		-1.2	V
t_{rr}	Body Diode Reverse Recovery Time	$I_F = -2\text{A}, di/dt = 100\text{A}/\mu\text{s}$	-	10	-	ns
Q_{rr}	Body Diode Reverse Recovery Charge		-	0.6	-	nC

- Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
 2. $R_{\theta JA}$ is measured with the device mounted on a 1inch^2 pad of 2oz copper FR4 PCB.
 3. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.

Typical Performance Characteristics

Figure 1: Power De-rating

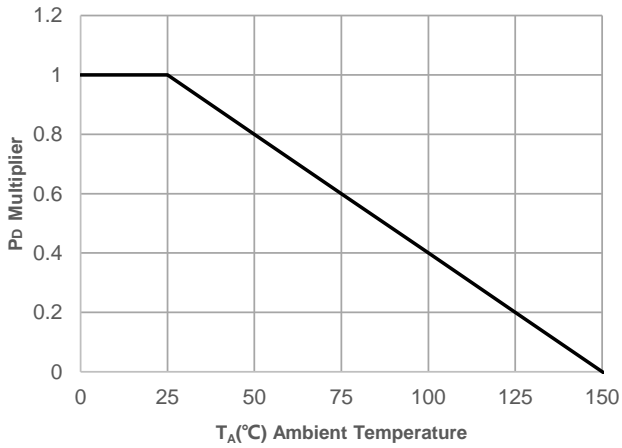


Figure 2: Current De-rating

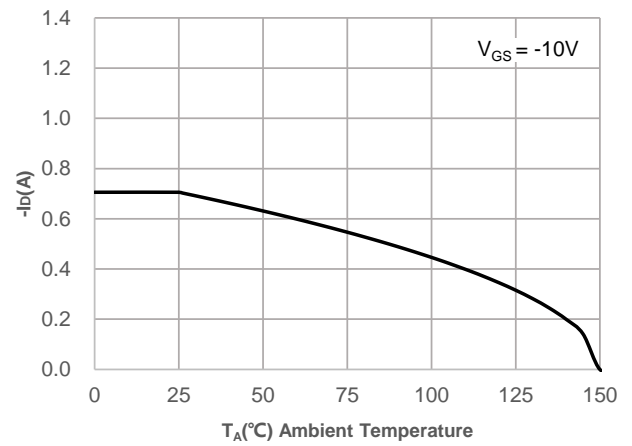


Figure 3: Normalized Maximum Transient Thermal Impedance

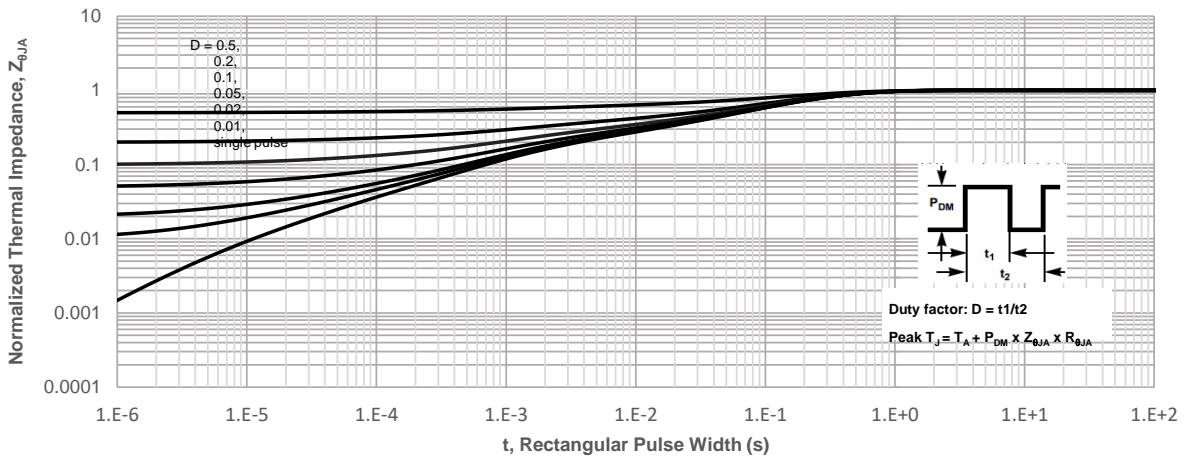
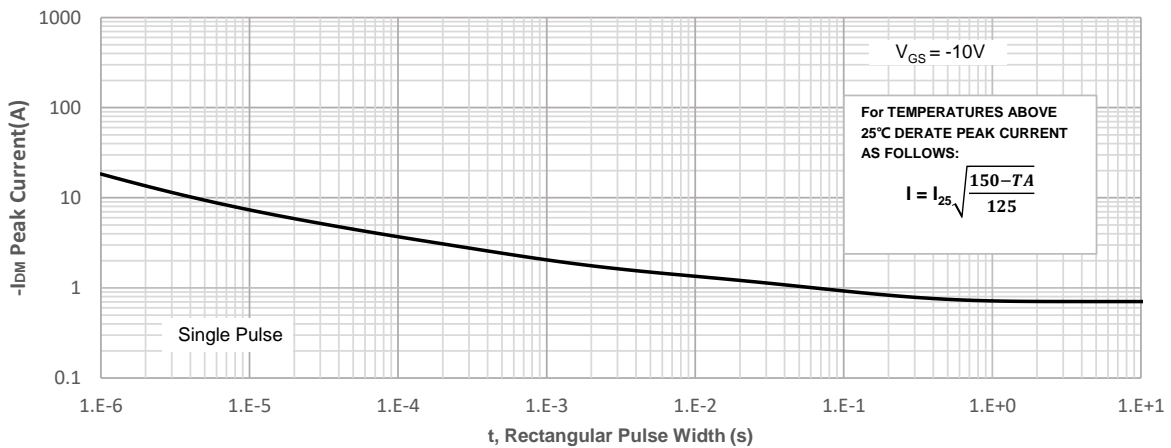
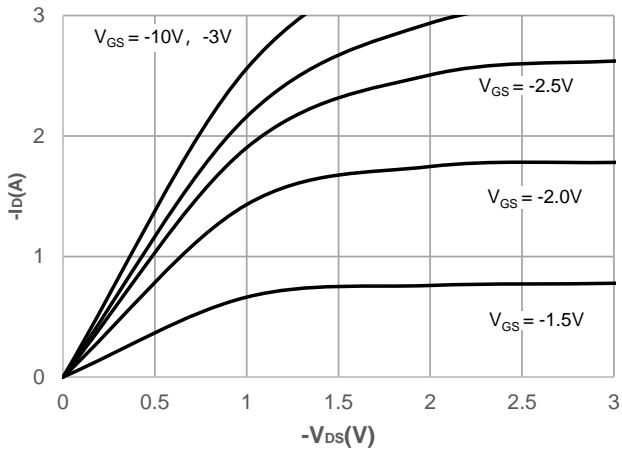
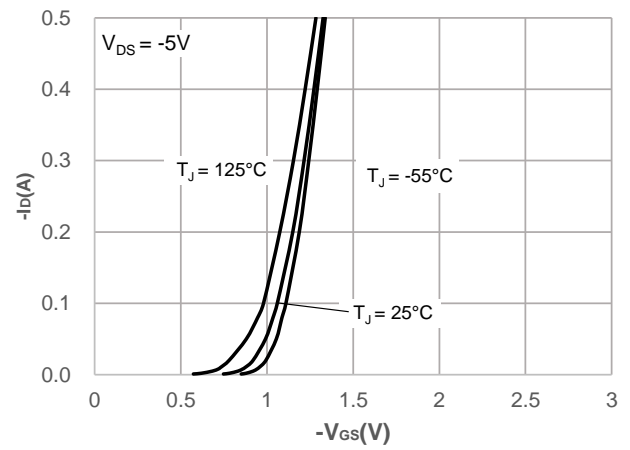
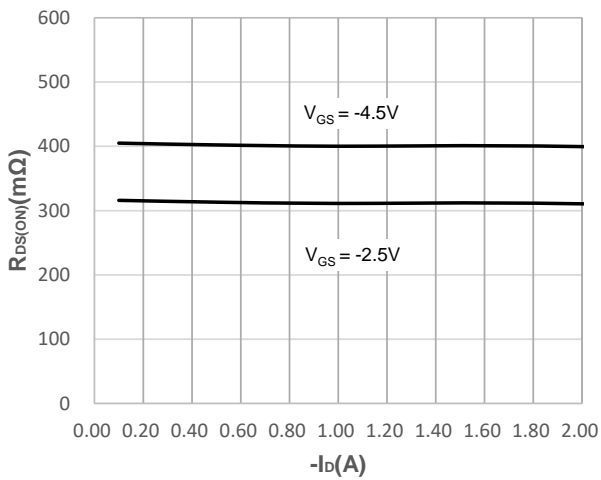
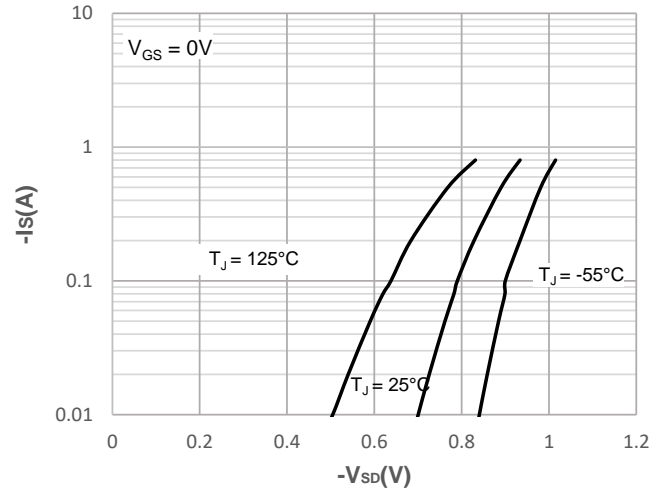
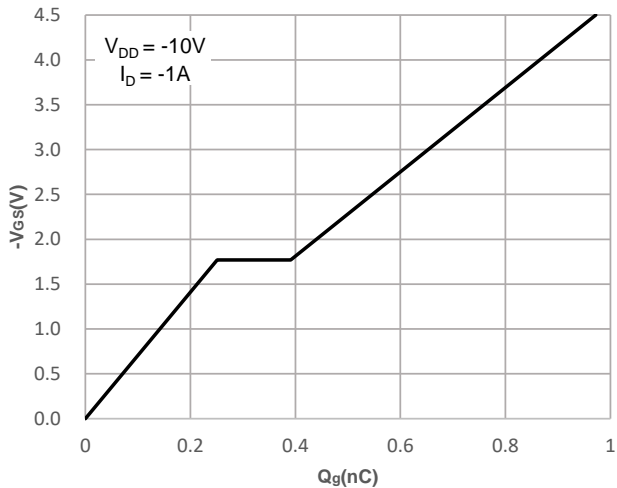
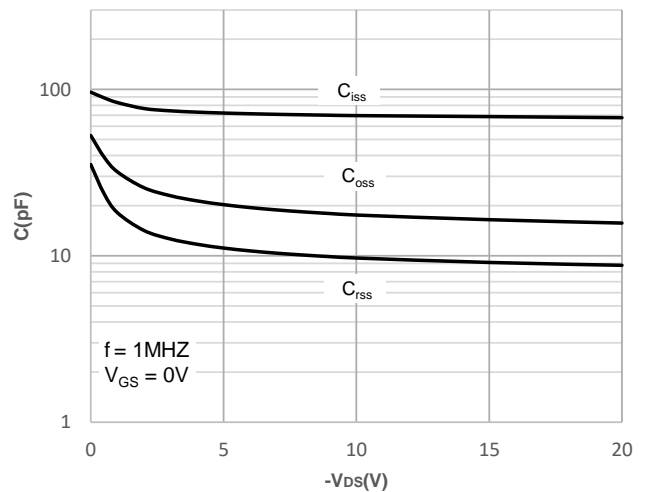


Figure 4: Peak Current Capacity



Typical Performance Characteristics

Figure 5: Output Characteristics

Figure 6: Typical Transfer Characteristics

Figure 7: On-resistance vs. Drain Current

Figure 8: Body Diode Characteristics

Figure 9: Gate Charge Characteristics

Figure 10: Capacitance Characteristics


Typical Performance Characteristics

Figure 11: Normalized Breakdown voltage vs. Junction Temperature

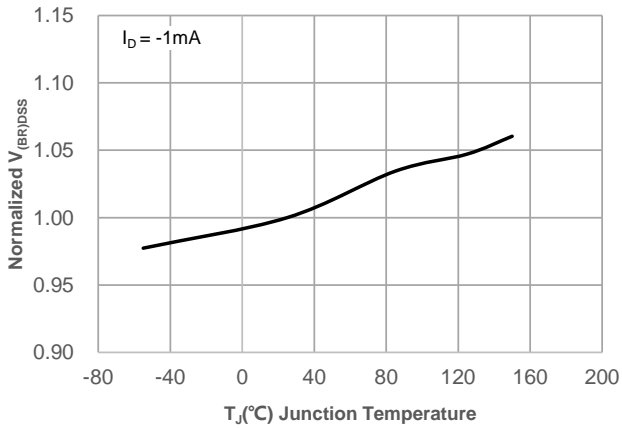


Figure 12: Normalized on Resistance vs. Junction Temperature

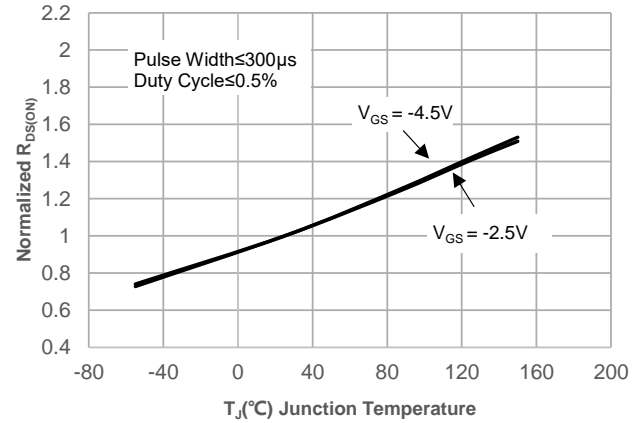


Figure 13: Normalized Threshold Voltage vs. Junction Temperature

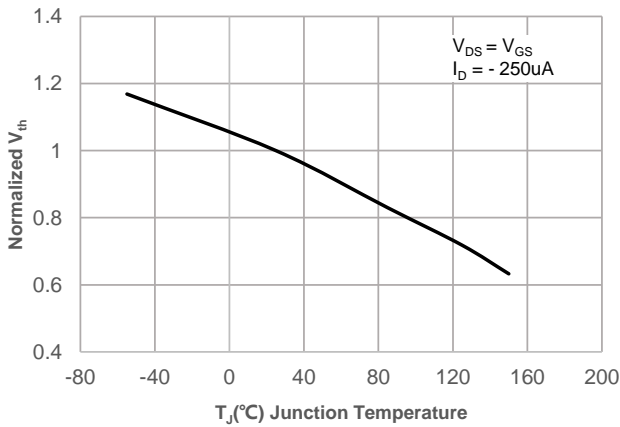


Figure 14: $R_{DS(ON)}$ vs. V_{GS}

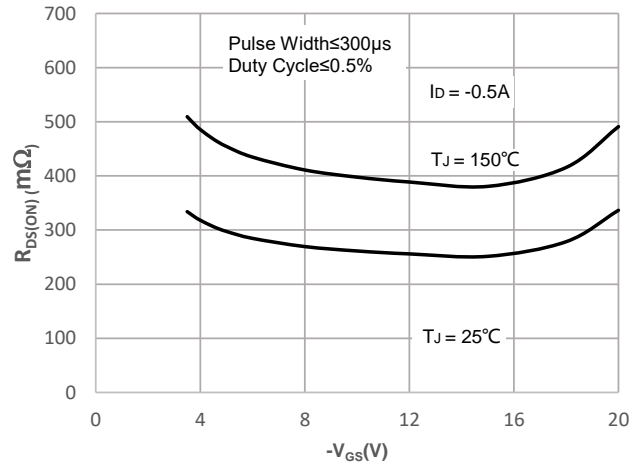
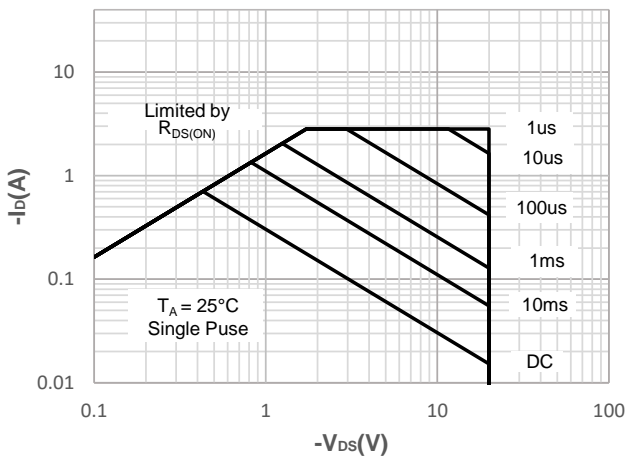
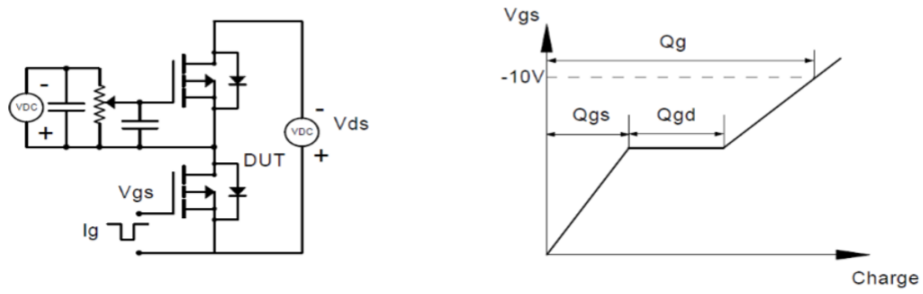
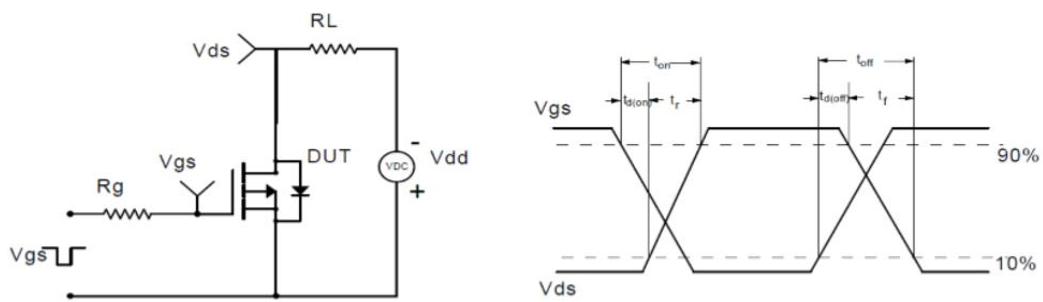
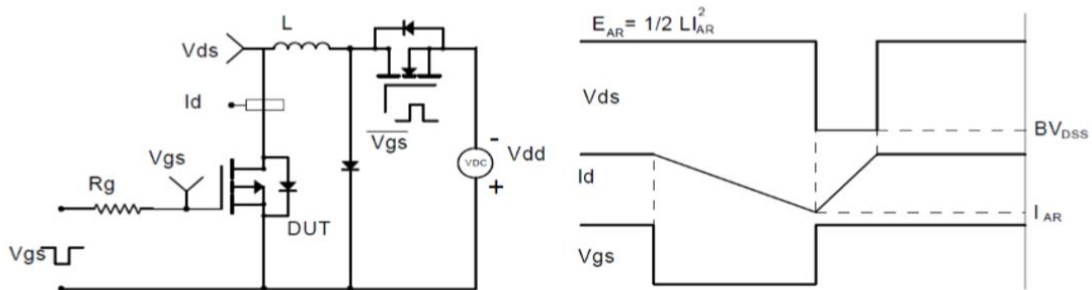
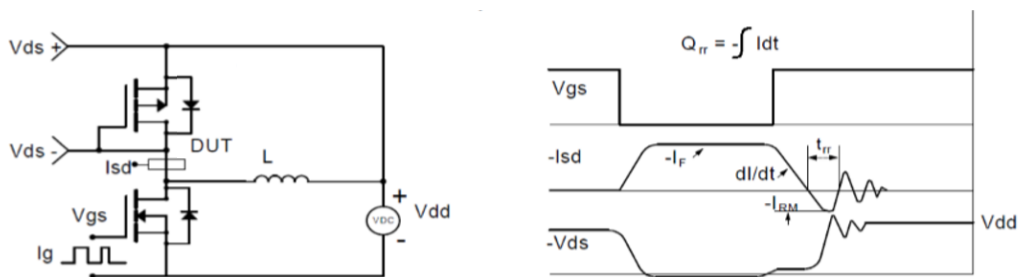


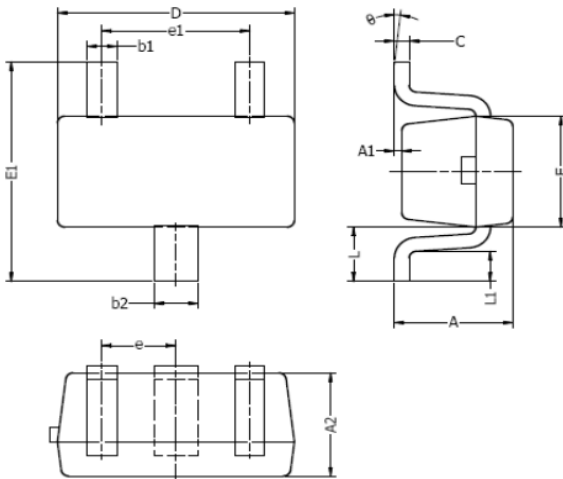
Figure 15: Maximum Safe Operating Area



Test Circuit

Figure 1: Gate Charge Test Circuit & Waveform

Figure 2: Resistive Switching Test Circuit & Waveform

Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

Figure 4: Diode Recovery Test Circuit & Waveform

Package Mechanical Data(SOT-523-3L)

Package Outline



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.70	0.90	0.028	0.035
A1	0.00	0.10	0.000	0.004
A2	0.70	0.80	0.028	0.031
b1	0.15	0.25	0.006	0.010
b2	0.25	0.35	0.010	0.014
c	0.10	0.20	0.004	0.008
D	1.50	1.70	0.059	0.067
E	0.70	0.90	0.028	0.035
E1	1.45	1.75	0.057	0.069
e	0.50 TYP.		0.020 TYP.	
e1	0.90	1.10	0.035	0.043
L	0.40 REF.		0.016 REF.	
L1	0.10	0.30	0.004	0.012
θ	0°	8°	0°	8°

NOTES:

1. Above package outline conforms to JEITA EAIJ ED-7500A SC-75A.
2. Dimensions are exclusive of Burrs, Mold Flash & Tie Bar extrusions.

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